Statistical Timing Graph Scheduling Algorithm for GPU Computation

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Introduction

Statistical Static Timing Analysis (SSTA) is a crucial technique in digital circuit design because it addresses on-chip variations by propagating timing distributions instead of fixed delays. However, the computational complexity of SSTA demands ***significant memory*** and ***long runtime***. While GPUs offer opportunities to accelerate SSTA, their ***limited memory capacity*** makes it challenging to handle large-scale SSTA workloads.

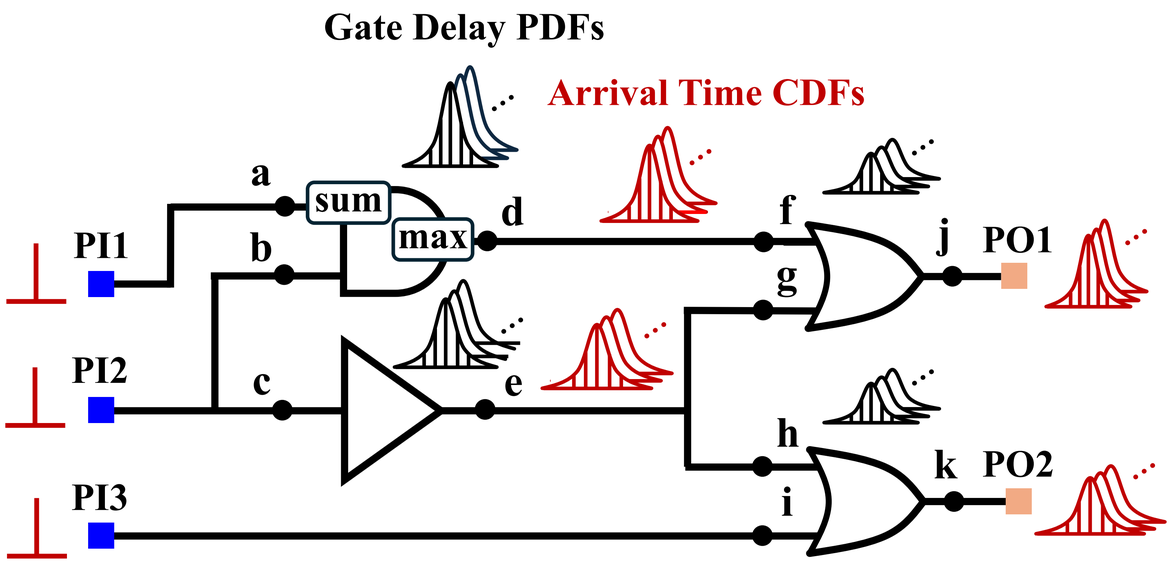


Figure 1: Illustration of a block-based SSTA problem.

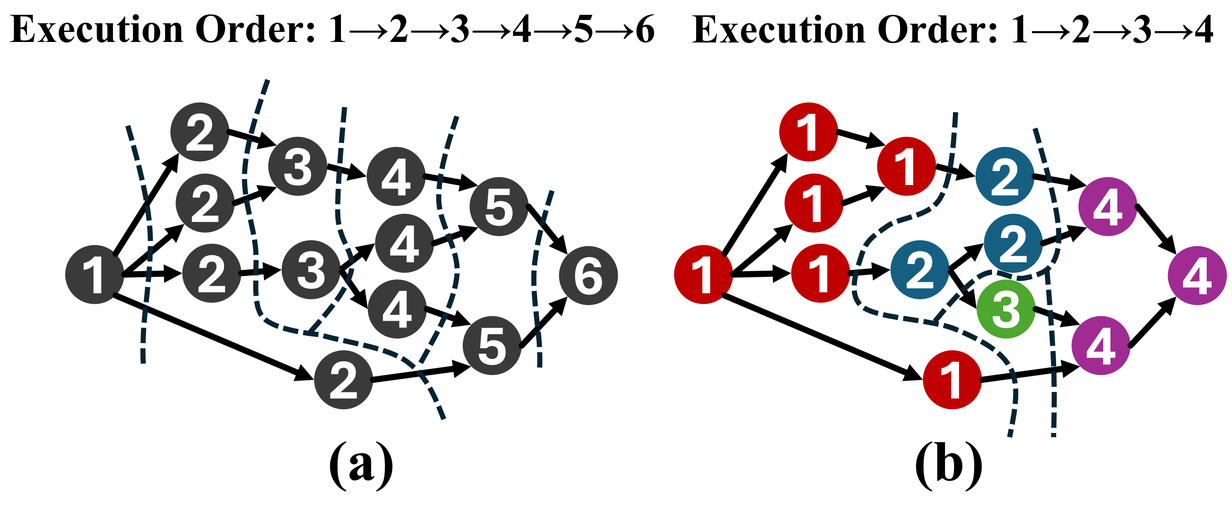
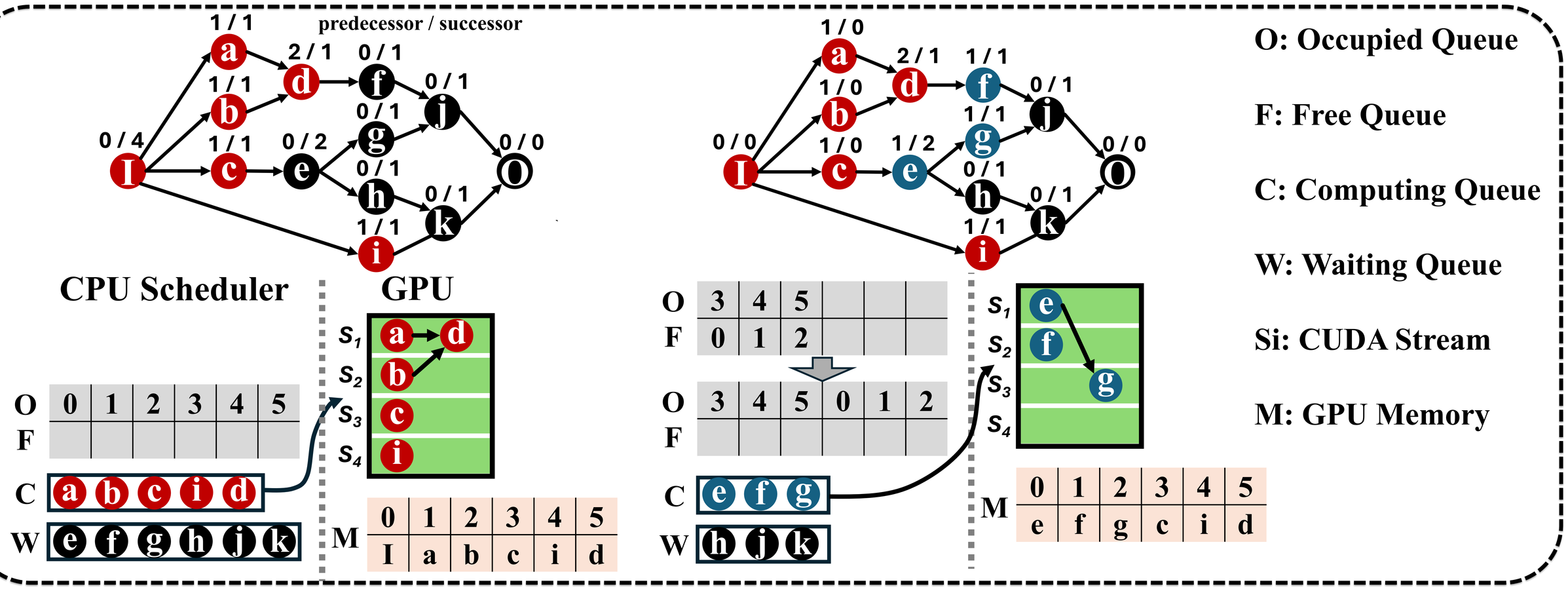


Figure 2: (a) The STG of the circuit (b) The scheduled STG for GPU.

Algorithm



Result

- **STG Generation**:
  - From OpenTimer, timing sampled $\sim\mathcal{N}(0,1)$
  - Circuit pins are assigned varying sizes
- **Baselines**:
  - Multi-threaded CPU Baseline (cpp)
  - CUDA Graphs GPU Baseline (cuf)
- **Experimental Setup**:
  - 20-thread CPU 128 GB RAM
  - NVIDIA GPU with 16 GB memory

Circuit	‖V‖ / ‖E‖	*Size*	*cpp*	*cuf*	*ours*
aes_core_1	66K / 86K	1.0	679	15405	370 (1.8×)
aes_core_2		2.0	1306	15599	450 (2.9×)
aes_core_3		3.1	1870	15576	396 (4.7×)
des_perf_1	303K / 387K	4.6	3106	OOM	1813 (1.7×)
des_perf_2		9.2	5798	OOM	2108 (2.7×)
des_perf_3		13.8	8474	OOM	1760 (4.8×)
vga_lcd_1	397K / 489K	6.0	4051	OOM	2367 (1.7×)
vga_lcd_2		12.1	7651	OOM	2271 (3.4×)
vga_lcd_3		18.2	11214	OOM	2297 (4.9×)

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